AS0216

LO generation and LO distribution path 2.5GHz-7.2GHz

DESCRIPTION

The ARGO Semi AS0216 IP is an LO generation and LO distribution path. The LO generation part receives an input clock signal in the range of 7.5-9.5GHz and through programmable division ratios and mixing it generates LO signals in the range of 3.8-7.6 GHz. The LO distribution path initially buffers the LO signal across long (several mm) chip lines and then generates I/Q LO signals to drive the Rx/Tx mixers. Depending on the desired frequency band, I/Q generation is obtained either through a delay-locked loop (on-frequency I/Q) or through a divide-by-2 circuit (I/Q at half frequency).
The cell maintains the close-in phase noise of the input clock signal while providing low noise floor and low level of generated spurs.

ABOUT ARGO SEMICONDUCTORS

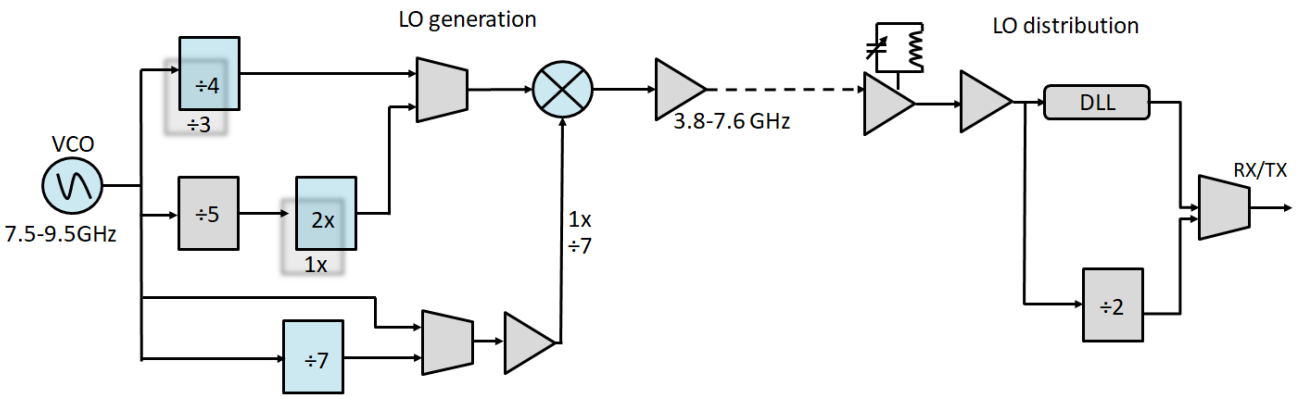
Argo Semiconductors offers high quality RF IP products operating in the frequency region between 2GHz and 10GHz. Argo's team has a long experience on Wi-Fi RF silicon product development and cellular RF silicon product development, bringing billions of chips to the market. Leveraging on these capabilities and building on its solid IP base, Argo helps its customers develop products that can meet the most stringent requirements, while shrinking the development time. IP customization is possible upon request.

APPLICATIONS

- WiFi6/6E-7
- Bluetooth
- CAT-1 SoC

FEATURES

- ✓ Programmable frequency up/down conversion
- ✓ Supply Voltage: 0.85V
- ✓ Input frequency: 7.5-9.5 GHz
- ✓ Output frequency: 2.4-7.2 GHz
- ✓ Technology node: GF 22FDX CMOS SOI
- ✓ Total area for 1 core: 3.5 mm^2



2.4 GHz : use {div5 + 2x} + div2
4.9 - 6.0 GHz : use {div3 or [div5 +2x]} + DLL
6.0 - 7.1 GHz : use {div4} + DLL

WLAN

3.0 - 3.8 GHz : use {div3 or div4 or div5} + div2
3.8 - 4.5 GHz : use {div3+div7} + DLL
4.5 - 4.9 GHz : use {div5 + 2x} + DLL

5GNR

Simplified Block Diagram

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Table 1: LOgen and LOdistr metrics

LOgen Characteristics						
Parameter		**Minimum**	**Typical**	**Maximum**	**Units**	**Comments**
Supply voltage			0.85		V	
Input frequency		7500		9500	MHz	
Output frequency		3800		7600	MHz	
Phase noise @ 6000 MHz	10 KHz		-125		dBc/Hz	fin=9000 MHz, includes LDO noise
	100 kHz		-129		dBc/Hz	
	1 MHz		-145		dBc/Hz	
	10 MHz		-157.5		dBc/Hz	
	100 MHz		-158.5		dBc/Hz	
Phase noise @ 5625 MHz	10 KHz		-128		dBc/Hz	fin=7500 MHz, includes LDO noise
	100 KHz		-130		dBc/Hz	
	1 MHz		-145		dBc/Hz	
	10 MHz		-157		dBc/Hz	
	100 MHz		-158.7		dBc/Hz	
Current consumption			14		mA	
Area			0.27		mm^2	includes LDO

LOdistr Characteristics						
Parameter		**Minimum**	**Typical**	**Maximum**	**Units**	**Comments**
Supply voltage			0.85		V	
Input frequency		3800		7600	MHz	
Output frequency		3800		7200	MHz	using DLL
		2400		3800		using DIV2
Phase noise @ 2400 MHz	10 KHz		-131		dBc/Hz	fin=4800 MHz, includes LDO noise
	100 KHz		-134		dBc/Hz	
	1 MHz		-147.4		dBc/Hz	
	10 MHz		-152		dBc/Hz	
	100 MHz		-155		dBc/Hz	
Current consumption			11		mA	
Area			0.28		mm^2	includes LDO